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Nonlinear Controller for the Set-Point Regulation of a Buck Converter System

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Abstract: In this paper, we present a nonlinear PID controller based on saturation functions with variable parameters in order to regulate the output voltage of a buck converter in the presence of changes in the input voltage. The main feature of the proposed controller is to bound the control input with a variable parameter to avoid the windup effect generated by the combination of the integral control action and some operation conditions. The main advantages of the proposed nonlinear PID controller are its low computing cost and the simple tuning task to implement the control strategy in an embedded system. The acceptable behavior of the closed-loop system is presented through the simulation and experimental results.

Keywords: nonlinear PID controller; buck converter; set-point regulation; simulation results

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1. Introduction

The control algorithms implemented in power electronic buck converters have improved the performance of this kind of system under nominal operation conditions, as explained in [1]. One of these nominal conditions is considered in the design process, namely that the input voltage remains constant during the entire operation. However, there are some systems, such as photovoltaics and wind turbines, where it is necessary to use the power electronic buck converter, but the main problem is the variable voltage produced by the temporal obstructions of the sun and wind speed variation, respectively. In some cases, the maximum power point tracking (MPPT) method has been applied to mitigate the above effect, however, this method is focused on maximizing the power output to various systems under different conditions, as described in [2].

In the literature, there are different control strategies to improve the behavior of power converters. For example, a robust optimal power management system for a micro-grid was explained in [3]. In [4], the authors described in detail how sliding mode controllers can be practically engineered to optimize the control of power converters. In [5], the fractional-order terminal sliding-mode control, which has a new fractional-order sliding surface and assures the finite time convergence of the output voltage error to the equilibrium point during the load changes, is presented. Other interesting approaches of the sliding mode control technique for the power electronic converter were explained in [6–10]. In [11], the

stability properties and results were given for the steady-state control error offset induced by stationary high-frequency measurement disturbances while operating the control loop close to saturation. In [12], the authors presented diverse alternative methods for the control of power electronic converters applying fractional order control. The controller was carried out by the design of a linear controller for the buck converter and the fractional calculus was proposed to determine the switching surface applying a fractional sliding mode control scheme to the control of such devices. In [13], a comparison between different techniques for the design and implementation of closed-loop control systems for buck converters was carried out. Controllers used for this comparison were integral, proportional plus integral controllers and artificial intelligence was represented in the fuzzy logic controller. Optimal switching between different topologies in step-down direct current–direct current (DC-DC) voltage converters, with non-ideal inductors and capacitors is presented in [14]. A backpropagation neural network to fit the input–output relationship of the offline control laws under different operating points was proposed in [15]. In [16], a mixed-logic dynamic model and control method based on mode selection were proposed for the buck converter. A novel fast model predictive control methodology based on linear parameter varying systems was explained in [17]. In [18], the authors presented a fuzzy logic controller that performs the output voltage regulation of a DC/DC buck power converter. Other interesting approaches of the fuzzy logic control technique for power electronic converters were explained in [19–21].

In general, most control strategies do not take into account changes in input voltage, which in combination with a control strategy with integral action, could produce the undesired windup effect in a buck converter. In other words, the windup effect refers to the situation in a PID controller where a large change between the set-point and the output system occurs for a relatively long time; consequently, the integral term accumulates a significant value and the specific problem is the excess overshooting. In [22], the main causes of this effect are described in the control context: the author explains that if the control contains integral action, input saturation can give rise to large and poorly decaying overshoots in the transients, which must be avoided. In the literature, there are control algorithms proposed to prevent the windup effect; for example, in [23], the authors focused on the anti-windup control problem for plants with input saturation, and a delayed decoupling structure was first proposed; then, appropriate linear matrix inequalities were developed to determine a plant-order anti-windup compensator. In [24], a unified framework was presented for the study of linear time-invariant systems subject to control input nonlinearities. The framework was based on the following design paradigm: designing the linear controller ignoring control input nonlinearities, and then adding anti-windup bumpless transfer compensation to minimize the adverse effects of any control input nonlinearities on closed-loop performance. In [25], a design method of robust disturbance feedback control was proposed by a linear matrix inequality, with industrial refrigeration system applications. The important aspects of anti-windup designs, namely the parametrization of linear anti-windup compensators, and the role of artificial nonlinearity in the design of anti-windup compensators for multivariable systems, were in presented [26].

The above control strategies improved the behavior of the buck converter; however, the simplicity to implement these controllers is an important topic for industrial applications. In this context, the proportional–integral–derivative controllers were the most adopted in industrial settings because of the advantageous cost–benefit ratio they are able to provide, as explained in [27]. Furthermore, in the literature, there are different variations of the proportional–integral–derivative controllers to improve the performance of the buck converter system. For example, in [28], the nonlinearity of a saturation was taken into account in a model of DC-DC buck power converters, for which a Lyapunov function-based class of proportional–integral with anti-windup algorithms was given. In [29], an internal model control-based anti-windup compensator was designed for nonlinear systems subjected to time-varying delay and input saturation. A robust nonlinear dynamic anti-windup compensator design for nonlinear systems with parametric uncertainties

and one-sided Lipschitz nonlinearities under actuator saturation was presented in [30]. In [31], we proposed a proportional–derivative controller with a saturation function where the parameters are variable, in order to improve the closed-loop system when there are time-variant disturbances; considering the previous work, we proposed a nonlinear PID controller to avoid the windup effect, which appears when the input voltage of the buck converter is time-variant. In summary, the contribution of this work focuses on:

- A novel nonlinear PID controller to avoid the windup effect;
- Simulation and experimental results to show the main advantage of the proposed controller;
- Comparative results between the behavior produced by classical PID and nonlinear PID controllers.

The paper is organized as follows. In Section 2, we describe the buck converter system and the design method to obtain its parameters. Section 3 presents the proposed nonlinear PID controller. The simulation results are given in Section 4. Finally, the conclusions and recommendations for future work are summarized in Section 5.

2. System Description

The buck converter system is a very simple type of DC-DC converter that produces an output voltage ($V_{out}(t)$) that is less than its input voltage ($V_{in}(t)$). In this section, we describe the general form of that the design process takes to obtain the parameter of the power electronic DC-DC converter and its behavior in the presence of changes in the input voltage. Figure 1 shows the topology of a buck converter, where it notices that this DC-DC converter is composed by a switch power (T_{MOSFET}), an inductance (L), a diode (d), a capacitor (C) and a load—in this case a resistance (R). The main goal of the buck converter is to regulate the capacitor voltage (V_c), where the load is connected, as for this the switch the power is manipulated by a pulse width modulation (PWM) signal with a constant period (T), as explained in [1].

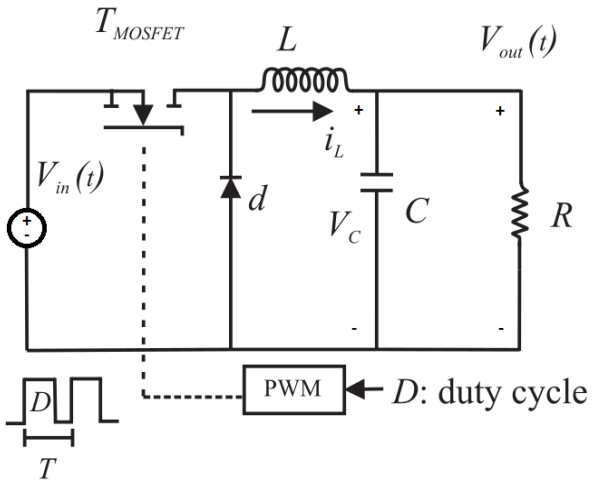

Figure 1. Topology of a buck converter system.

Then, taking into account the general equations for the process design of a buck converter system, as explained in [1], we obtained the parameters that are shown in Table 1, assumed that the system is operating under nominal conditions.

Table 1. Buck converter parameters.

$V_{in}(t)$	=	12 V	P_{load}	=	0.81 W	C =	3.6×10^{-5} F
$V_{out}(t)$	=	9 V	D	=	0.75	L =	3.1×10^{-3} H
$\Delta V_{out}(t)$	=	0.1 V	f	=	5 KHz	R =	100 Ω

Now, in order to validate the obtained parameters, for a buck converter system, we performed the simulation using the *Simscape* libraries of Matlab-Simulink, with $V_{in}(t) = 12$ V. The output voltage of the buck converter system with 75% of PWM signal duty cycle is $D = 0.75$, as shown in Figure 2. Observe that the output voltage $V_{out}(t)$ converges to the desired value—which is $V_d = 9$ V. Furthermore, notice that in the beginning, there is an overshoot by which we could avoid changing the resistance value by a lower one, but as a consequence, the power increases—more details can be found in [1]. Then, to retain the design power, we will keep the obtained parameters.

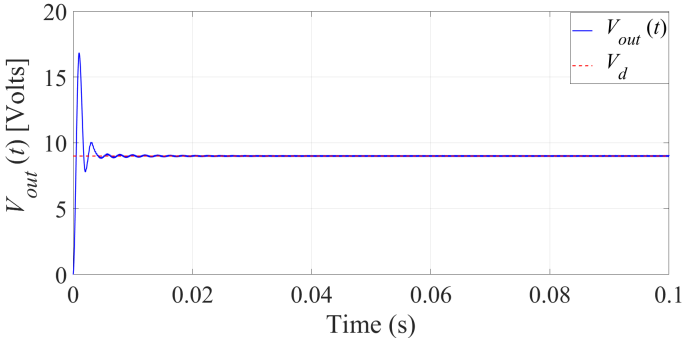

Figure 2. Output voltage ($V_{out}(t)$) of the buck converter system with a constant input voltage ($V_{in}(t)$).

In general, the performance of the buck converter is acceptable from a practical point of view. Now, in order to show the buck converter behavior, with a constant PWM signal duty cycle, the input voltage ($V_{in}(t)$) changes as follows:

$$V_{in}(t) = \begin{cases} 12 \text{ V} & if \quad t \leq 0.02 \text{ s} \\ 11 \text{ V} & if \quad 0.02 < t \leq 0.05 \text{ s} \\ 6 \text{ V} & if \quad 0.05 < t \leq 0.07 \text{ s} \\ 12 \text{ V} & if \quad 0.07 < t \text{ s} \end{cases} \tag{1}$$

where the values were arbitrarily chosen, considering that in a time interval $V_{in}(t)$ is smaller than V_d. In Figure 3, we observe the obtained output voltage ($V_{out}(t)$) when $V_{in}(t)$ is an input time-varying voltage, and notice that the behavior is degraded. Therefore, we propose a control algorithm for the case of the set-point regulation of the buck converter output voltage when there is an input time-varying voltage.

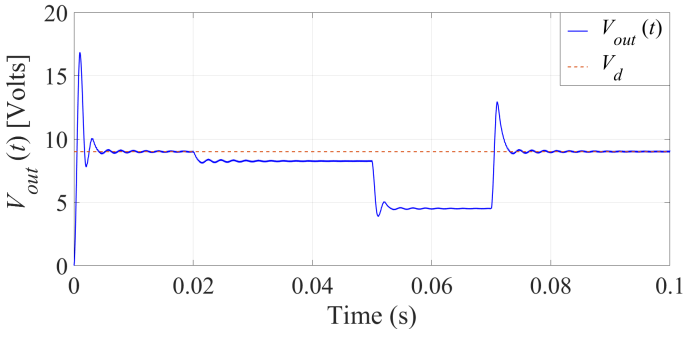

Figure 3. Output voltage ($V_{out}(t)$) of the buck converter system with input time-varying voltage ($V_{in}(t)$).

Notice that, normally, the buck converter system is operated with a constant input voltage; however, when $V_{in}(t)$ is obtained from a wind turbine or a photovoltaic power sys-

tem, the input voltage could be variable, then a control algorithm is needed to manipulate the duty cycle of the PWM signal to obtain the desired output voltage.

3. Control Strategy

A possible solution to improve the behavior of the buck converter, when there is an input time-varying voltage, is to manipulate the PWM signal duty cycle with a control strategy. In Figure 4, note that the diagram of the buck converter system with control action is in this case a closed-loop system.

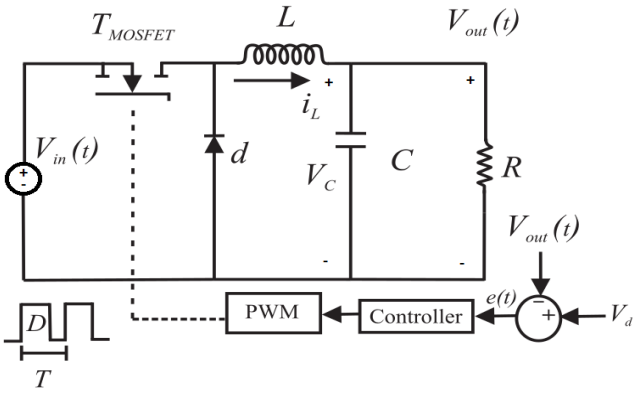

Figure 4. Buck converter with an control action (closed-loop system).

There are a wide variety of control strategies that have been implemented in a buck converter system as we described in the Introduction section. However, proportional–integral–derivative (PID) controllers are the most adopted in industrial settings because of the advantageous cost–benefit ratio they are able to provide. The mathematical expression of a classical PID controller is given by the following equation:

$$U_{PID} = k_1 e(t) + k_2 \int_0^t e(\tau) d\tau + k_3 \frac{de(t)}{dt} \tag{2}$$

where k_1, k_2, k_3 represent the proportional, integral and derivative gains, respectively, and $e(t)$ represents the error, which is defined as

$$e(t) = V_d - V_{out}(t) \tag{3}$$

The PID controller has the disadvantage that under some operation conditions, this controller generates the windup effect. In the case of the buck converter, this effect is produced when the input voltage ($V_{in}(t)$) is smaller than the desired voltage (V_d) in a interval time, as the example that we show in Equation (1), when $V_{in}(t) = 6$ V in the interval time $t \in (0.05, 0.07]$ s, such that the integral term increases to a relatively large value.

Consequently, we propose implementing a nonlinear PID controller based on saturation functions with variable parameters, which has the same advantage as the classical PID controller, a low computing cost and a simple tuning task to implement the control strategy in an embedded system, but in addition, the nonlinear PID controller also avoids the windup effect. Then, let $\sigma_{\bar{b}_i}(k_i h_i)$ be a saturation function for $i = 1, 2, 3$; notice that $\bar{b}_i$ and k_i are constant and also positive definite, given by the following equation:

$$\sigma_{\bar{b}_i}(k_i h_i) = \begin{cases} \bar{b}_i & if \quad k_i h_i > \bar{b}_i \\ k_i h_i & if \quad \mid k_i h_i \mid \leq \bar{b}_i \\ -\bar{b}_i & if \quad k_i h_i < -\bar{b}_i \end{cases} \tag{4}$$

where k_i is the gain, and $\bar{b_i}$ is the parameter chosen to limit the values of any function represented by h_i. Observe that h_1, h_2 and h_3 represent the error, its integral and derivative, respectively. Then, in order to improve the behavior of the closed-loop system and to avoid the windup effect, the PID controller defined by Equation (2) can be modified by implementing the above saturation functions in each term, as follows:

$$U_{NLPID} = \sigma_{\bar{b_1}}[k_1 e(t)] + \sigma_{\bar{b_2}}[k_2 \int_0^t e(\tau)d\tau] + \sigma_{\bar{b_3}}[k_3 \frac{de(t)}{dt}] \tag{5}$$

Now, Equation (5) can be rewritten in a compact form as

$$U_{NLPID} = \sum_{i=1}^{3} u_i \tag{6}$$

where $u_i = \sigma_{\bar{b_i}}(k_i h_i)$ for $i = 1, 2, 3$; represents the saturation of the proportional, integral and derivative control action, respectively. Then, applying Equation (4) we can rewrite u_i as follows:

$$u_i = \begin{cases} sign(h_i)\bar{b_i} & if \quad |k_i h_i| > \bar{b_i} \\ k_i h_i & if \quad |k_i h_i| \leq \bar{b_i} \end{cases} \tag{7}$$

To introduce a modification of saturations (7), let us consider the point of h_i where $|u_i| = \bar{b_i}$, which is:

$$|u_i| = |k_i h_i| = \bar{b_i} \implies |h_i| = \bar{b_i}/k_i \tag{8}$$

then, we define:

$$d_i := \bar{b_i}/k_i \tag{9}$$

as consequence, we have that:

$$u_i = sign(h_i)\bar{b_i} \quad \forall \quad |h_i| > d_i \tag{10}$$

According to Equations (9) and (10), we can express (7) as follows:

$$u_i = \begin{cases} sign(h_i)\bar{b_i} & if \quad |h_i| > d_i \\ \bar{b_i} d_i^{-1} h_i & if \quad |h_i| \leq d_i \end{cases} \tag{11}$$

where the tuning parameters of the controller are b_i and d_i, $\forall\ i = 1, 2, 3$. To express Equation (11) in terms of h_i, when $|h_i| > d_i$, we consider that:

$$sign(h_i)\bar{b_i} = h_i sign(h_i)\bar{b_i} h_i^{-1} \tag{12}$$

then:

$$sign(h_i)\bar{b_i} = |h_i|\bar{b_i} h_i^{-1} \tag{13}$$

and considering that $|h_i|h_i^{-1} = |h_i|^{-1}h_i$, then Equation (11) can be rewritten as

$$u_i = \begin{cases} \bar{b_i}|h_i|^{-1}h_i & if \quad |h_i| > d_i \\ \bar{b_i} d_i^{-1} h_i & if \quad |h_i| \leq d_i \end{cases} \tag{14}$$

Finally, the law control given by Equation (5) can be represented as

$$U(t) = u_1 + u_2 + u_3 = k_1(\cdot)e(t) + k_2(\cdot)\int_0^t e(\tau)d\tau + k_3(\cdot)\frac{de(t)}{dt} \tag{15}$$

with:

$$k_1(\cdot) = \begin{cases} \bar{b_1}|e(t)|^{-1} & if \quad |e(t)| > d_1 \\ \bar{b_1} d_1^{-1} & if \quad |e(t)| \leq d_1 \end{cases} \tag{16}$$

$$k_2(\cdot) = \begin{cases} \bar{b_2}|\int_0^t e(\tau)d\tau|^{-1} & if \quad |\int_0^t e(\tau)d\tau| > d_2 \\ \bar{b_2}d_2^{-1} & if \quad |\int_0^t e(\tau)d\tau| \leq d_2 \end{cases} \tag{17}$$

$$k_3(\cdot) = \begin{cases} \bar{b_3}|\frac{de(t)}{dt}|^{-1} & if \quad |\frac{de(t)}{dt}| > d_3 \\ \bar{b_3}d_3^{-1} & if \quad |\frac{de(t)}{dt}| \leq d_3 \end{cases} \tag{18}$$

The advantage of this controller is that the gains change in function of the error, its integral and derivative action; however, in a small region defined by the parameters $\bar{b_i}$ and d_i, these gains are constant. Therefore, it is easy to choose the parameters $\bar{b_i}$ and d_i taking into account the region where k_i is a constant value. However, the maximum control input value is limited by the parameters $\bar{b_1}$, $\bar{b_2}$ and $\bar{b_3}$; thus, in order to override this limitation, we propose that the saturation parameter $\bar{b_i}$, from Equation (14), changes as follows:

$$\bar{b_i} = \begin{cases} b_i|h_i|^{\mu_i} & if \quad |h_i| > d_i \\ b_i|d_i|^{\mu_i} & if \quad |h_i| \leq d_i \end{cases} \tag{19}$$

$$\forall i = 1, 2, 3 \text{ and } \mu_i \in [0, 1].$$

Then, by introducing Equation (19) into Equation (14) we obtain:

$$u_i = \begin{cases} b_i|h_i|^{\mu_i}|h_i|^{-1}h_i & if \quad |h_i| > d_i \\ b_i|d_i|^{\mu_i}d_i^{-1}h_i & if \quad |h_i| \leq d_i \end{cases} \tag{20}$$

$$\forall i = 1, 2, 3 \text{ and } \mu_i \in [0, 1].$$

Consequently, from Equation (20), we obtain a nonlinear PID controller as follows:

$$U_{NLPID} = u_1 + u_2 + u_3 = k_1(\cdot)e(t) + k_2(\cdot)\int_0^t e(\tau)d\tau + k_3(\cdot)\frac{de(t)}{dt} \tag{21}$$

with:

$$k_1(\cdot) = \begin{cases} b_1|e(t)|^{(\mu_1-1)} & if \quad |e(t)| > d_1 \\ b_1d_1^{(\mu_1-1)} & if \quad |e(t)| \leq d_1 \end{cases} \tag{22}$$

$$k_2(\cdot) = \begin{cases} b_2|\int_0^t e(\tau)d\tau|^{(\mu_2-1)} & if \quad |\int_0^t e(\tau)d\tau| > d_2 \\ b_2d_2^{(\mu_2-1)} & if \quad |\int_0^t e(\tau)d\tau| \leq d_2 \end{cases} \tag{23}$$

$$k_3(\cdot) = \begin{cases} b_3|\frac{de(t)}{dt}|^{(\mu_3-1)} & if \quad |\frac{de(t)}{dt}| > d_3 \\ b_3d_3^{(\mu_3-1)} & if \quad |\frac{de(t)}{dt}| \leq d_3 \end{cases} \tag{24}$$

$$\forall \mu_1, \mu_2, \mu_3 \in [0, 1].$$

Notice that the controller obtained in Equation (21) is the proposed PID controller based on saturation functions with variable parameters, which we called the nonlinear PID controller. To show the behavior of the variable gains given by Equations (22)–(24), we plotted an example considering that the error value $(e(t))$ is increases from -50 to 50 in 100 s, with $\mu_1 = \mu_2 = 0$, $d_1 = 5$, $b_1 = 100$, $d_2 = 100$, $b_2 = 150$ and the derivative error value increasing from -25 to 25 in 50 s, with $\mu_3 = 0$, $d_3 = 5$, $b_3 = 100$—as shown in Figure 5a–c, respectively.

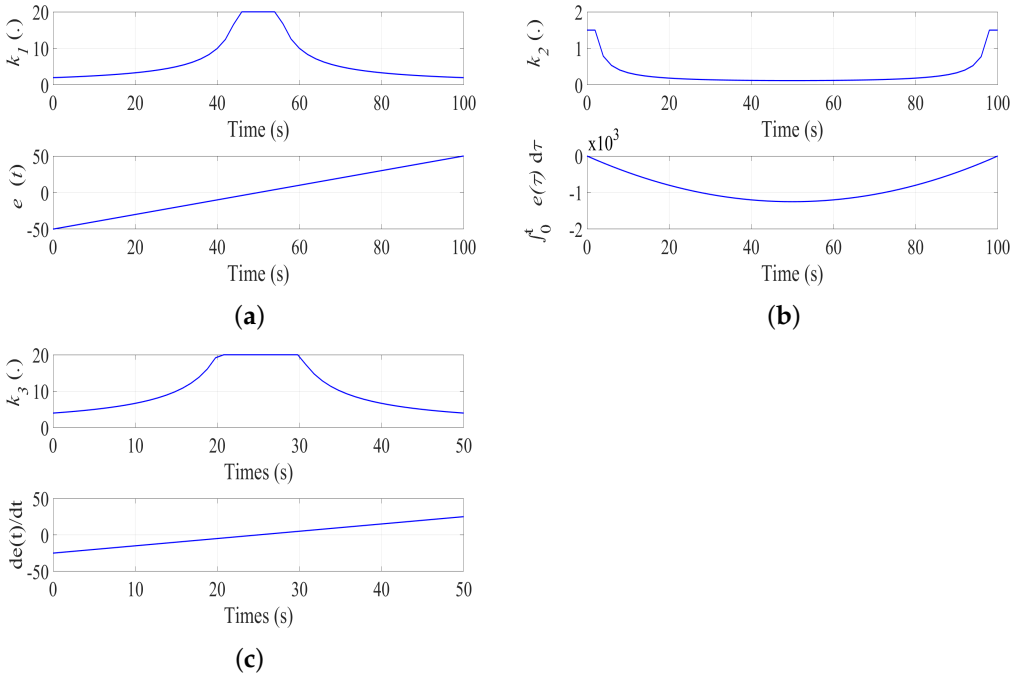

Figure 5. Plot of a variable gain obtained by Equations (22)–(24).

4. Closed-Loop System Simulation

The control strategy described in the previous section was implemented in a power electronic buck converter to generate the PWM signal duty cycle, which manipulates the state of the switch power and consequently the output voltage ($V_{out}(t)$), as depicted in Figure 4. In order to show the main advantage of the proposed nonlinear PID controller, given by Equation (21), we also performed the simulation of the closed-loop system implemented in the classical PID controller given by Equation (2) in the following scenarios:

- SCENARIO 1: Low-input voltage for a short time.
  In this scenario, we consider that the input time-varying voltage ($V_{in}(t)$) is under the desired value for a relatively short time, in this case 0.02 s.
- SCENARIO 2: Low-input voltage for a long time.
  In this scenario, we consider that the input time-varying voltage ($V_{in}(t)$) is under the desired value for a relatively long time—for this case 10 s.

4.1. SCENARIO 1: Low-Input Voltage for a Short Time

The simulation of this scenario was performed considering the input voltage ($V_{in}(t)$) defined by Equation (1). In [32], the author explained different methods to tuning a PID controller; however, the gains for both controllers were adjusted, taking into account the root-mean-square error of the output voltage ($RMSE_{V_{out}(t)}$), the steady state error (SSE) and settling time (ST), in order to improve the performance of the closed-loop system. In order to compare the behavior of the closed-loop system implementing the proposed nonlinear PID controller with respect to the classical PID controller, in this scenario, we performed three simulations for the case of the set-point regulation of the output voltage: the first and second show the performance obtained by implementing a classical PID controller for different gains' values, while the third simulation shows the closed-loop system's performance using the proposed nonlinear PID controller. The gains for the classical PID and the nonlinear PID controllers are shown in Tables 2 and 3, respectively.

Table 2. Gains for a classical PID controller.

Simulation 1	$k_1 = 6$	$k_2 = 12$	$k_3 = 0.0009$
Simulation 2	$k_1 = 1000$	$k_2 = 1500$	$k_3 = 0.1$

Table 3. Gains for a nonlinear PID controller.

For k_1	$b_1 = 200$	$d_1 = 0.1$	$\mu_1 = 0.01$
For k_2	$b_2 = 170$	$d_2 = 0.1$	$\mu_2 = 0.005$
For k_3	$b_3 = 0.1$	$d_3 = 0.1$	$\mu_3 = 0.9$

For the case of the classical PID controller, we performed two simulations: in the first simulation, we used relatively small gains obtained during the tuning task. In the second simulation, we increased the gains in order to improve the obtained steady state error value.

In Figure 6, we observe the output voltage produced by the buck converter system when a classical PID controller is implemented: the gains used in this simulation are shown in Table 2 as simulation 1. The obtained results of this simulation are: $RMSE_{V_{out}(t)} = 1.4722$ V, $SSE = 0.1383$ V and $ST = 0.0013$ s; from a practical point of view, the obtained SSE value is acceptable. However, to improve this result, we performed a second simulation, adjusting the classical PID controller gains.

The PWM signal duty cycle generated by the classical PID controller (U_{PID}) is shown in Figure 7. Notice that the magnitude of the PWM signal duty cycle is bigger than acceptable values of D: it is $D \in [0, 1]$. Consequently, the PWM block, depicted in Figure 4, has the following constraints: $D = 0$ if $U_{PID} \leq 0$, $D = 1$ if $1 \leq U_{PID}$ and $D = 0.5$ if $V_{in}(t) < V_d$.

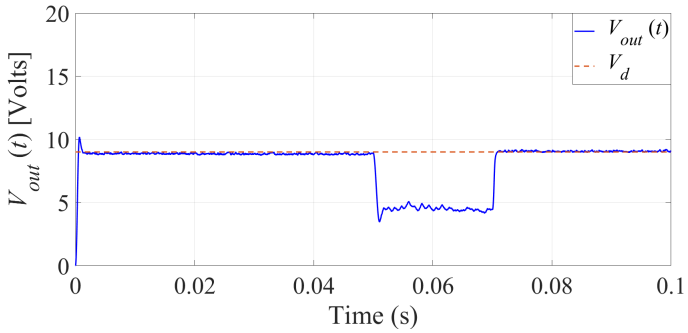

Figure 6. Scenario 1: Output voltage ($V_{out}(t)$) implementing a classical PID controller (simulation 1).

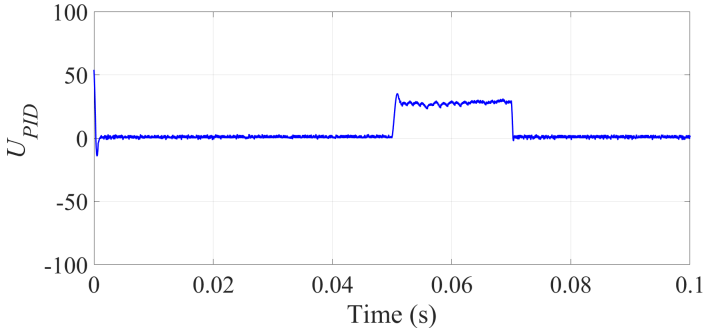

Figure 7. Scenario 1: Control input to generate the duty cycle of a PWM signal using a classical PID controller (simulation 1).

Now, for the second simulation, the used gains of the classical PID controller are shown in Table 2 as simulation 2. In Figure 8, we observe the behavior of the output voltage with the following results: $RMSE_{V_{out}(t)} = 1.5314$ V, $SSE = 0.0881$ V and $ST = 0.0019$ s. We note that the SSE value is improved; nevertheless, the obtained $RMSE_{V_{out}(t)}$ and ST are bigger than the previous results given the overshoot produced by the increase in the input control, as shown in Figure 9.

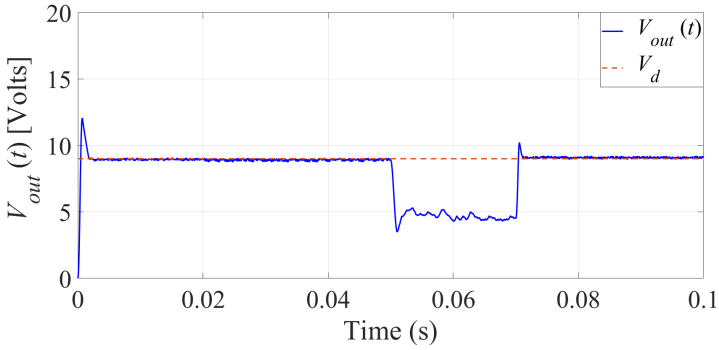

Figure 8. Scenario 1: Output voltage ($V_{out}(t)$) implementing a classical PID controller (simulation 2).

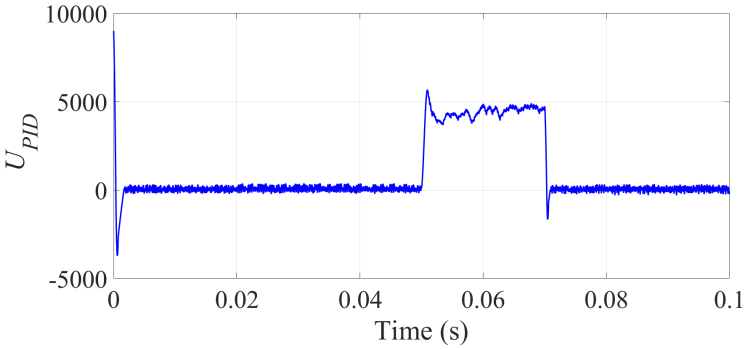

Figure 9. Scenario 1: Control input to generate the duty cycle of a PWM signal using a classical PID controller (simulation 2).

In Figure 10, we observe that the output voltage ($V_{out}(t)$), produced by implementing the proposed nonlinear PID controller, converges to desired value (V_d) when $V_{in}(t) \geq V_d$ with the following results: $RMSE_{V_{out}(t)} = 2.3313$ V, $SSE = 0.0533$ V and $ST = 0.0018$ s. We note that, in this case, the obtained SSE value is improved, however, the $RMSE_{V_{out}(t)}$ is bigger than the previous obtained values given the implementation of the saturation functions with variable parameters in the proposed controller.

The value of the PWM signal duty cycle (D), generated by Equation (21), is shown in Figure 11. Notice that the magnitude of the PWM signal duty cycle is bigger than any acceptable values of D, as it is $D \in [0, 1]$. However, the PWM block, depicted in Figure 4, has the following constraints: $D = 0$ if $U_{NLPID} \leq 0$, $D = 1$ if $1 \leq U_{NLPID}$ and $D = 0.5$ if $V_{in}(t) < V_d$. Even though D is bounded, the behavior of the PWM signal duty cycle, generated by the proposed controller, has influenced the dynamics of the system.

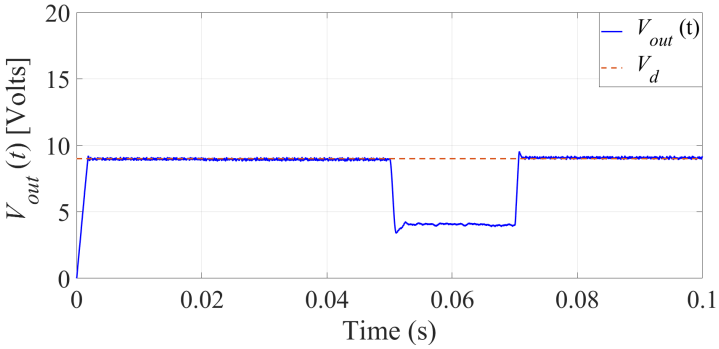

Figure 10. Scenario 1: Output voltage ($V_{out}(t)$) implementing the proposed nonlinear PID controller.

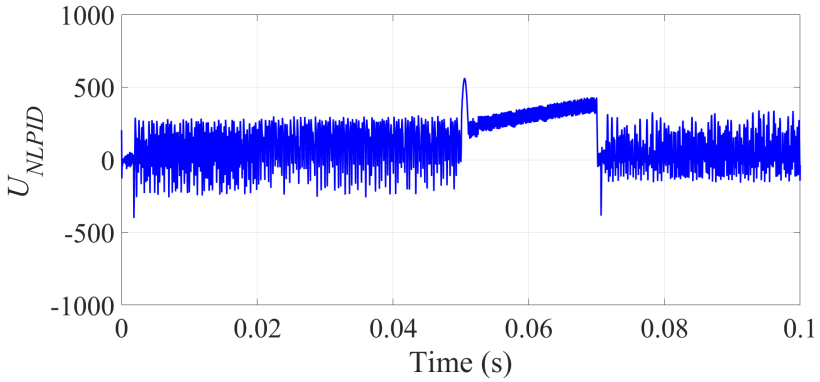

Figure 11. Scenario 1: Control input to generate the duty cycle of a PWM signal using the proposed nonlinear PID controller.

In summary, the obtained $RMSE_{V_{out}(t)}$, SSE and ST values of each simulation are shown in Table 4, where we observe that the proposed nonlinear PID controller has the smallest SSE value. In this scenario, there are no significant advantages of using the proposed nonlinear PID controller; however, in the following scenario, the windup effect in the output voltage is considered to evaluate the performance of the closed-loop system implementing both controllers.

Table 4. System performance for scenario 1.

Controller	$RMSE_{V_{out}(t)}$ (Volts)	SSE (Volts)	ST (s)
Classical PID (Simulation 1)	1.4722	0.1383	0.0013
Classical PID (Simulation 2)	1.5314	0.0881	0.0019
Nonlinear PID	2.3313	0.0533	0.0018

4.2. SCENARIO 2: Low-Input Voltage for a Long Time

In this scenario, we tested both the controller with exactly the same gains that we implemented in the previous scenario, but with the input voltage defined by the follow equation:

$$V_{in}(t) = \begin{cases} 12\text{ V} & if \quad t \leq 10\text{ s} \\ 6\text{ V} & if \quad 10 < t \leq 20\text{ s} \\ 12\text{ V} & if \quad 20 < t\text{ s} \end{cases} \tag{25}$$

where we note that the input voltage, in the interval time from 10 to 20 s, is smaller than the desired voltage. This operation condition was chosen in order to test the robustness of the proposed nonlinear PID controller. Consequently, in order to evaluate the performance of the closed-loop system, implementing both controllers, we obtained the $RMSE_{V_{out}(t)}$, SSE and ST values after the input voltage disturbance, which is for 20 < t seconds.

For practical reasons, we first present the results obtained by implementing the classical PID controller with the gains used in simulation 1 of scenario 1, which were significantly less than the gains used in simulation 2; then, we performed a new simulation implementing the classical PID controller with $k_1 = 6$, $k_2 = 12$ and $k_3 = 0.009$ under the conditions of input voltage defined in Equation (25). In Figure 12, notice that the windup effect is presented even though we used the relative small gains; in this case, the obtained results are: $RMSE_{V_{out}(t)} = 1.5726$ V, $SSE = 0.0499$ V and $ST = 15$ s. In Figure 13, we observe the increase in the input controller with respect to the obtained result shown in Figure 7.

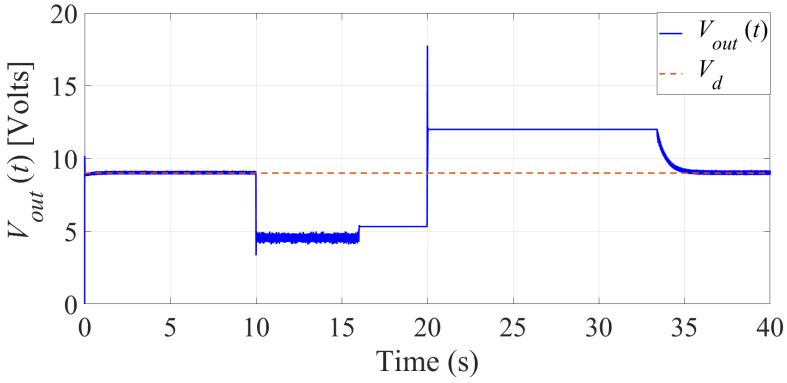

Figure 12. Scenario 2: Output voltage ($V_{out}(t)$) implementing a classical PID controller (simulation 1).

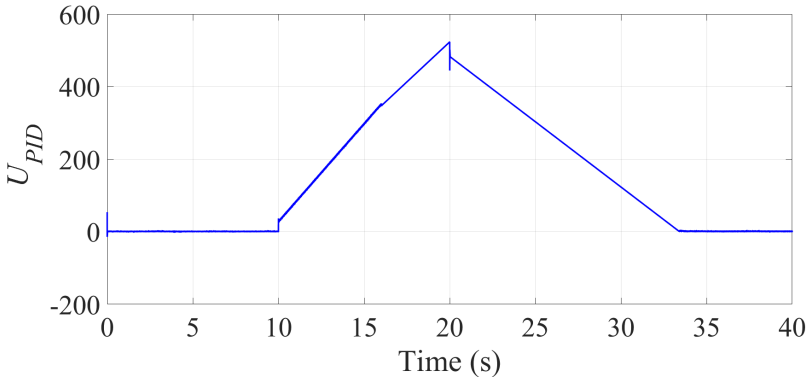

Figure 13. Scenario 2: Control input to generate the duty cycle of a PWM signal using a classical PID controller (simulation 1).

Now, implementing the gains used in simulation 2 of scenario 1, these being $k_1 = 1000$, $k_2 = 1500$, and $k_3 = 0.1$, we obtained results similar to those of the previous simulation. In Figure 14, we observe that the buck converter output voltage ($V_{out}(t)$) presents the windup effect, given that the PWM signal duty cycle, generated by the classical PID controller, is increasing by the integral term, as shown in Figure 15. Consequently, after $t = 20$, the output voltage converges towards the desired value in approximately $ST = 13$ seconds and the $RMSE_{V_{out}(t)}$ value has increased to 1.6126 V and we obtain a similar value for SSE—which is 0.432. Notice that the ST value was degraded with respect to the obtained result of the scenario 1.

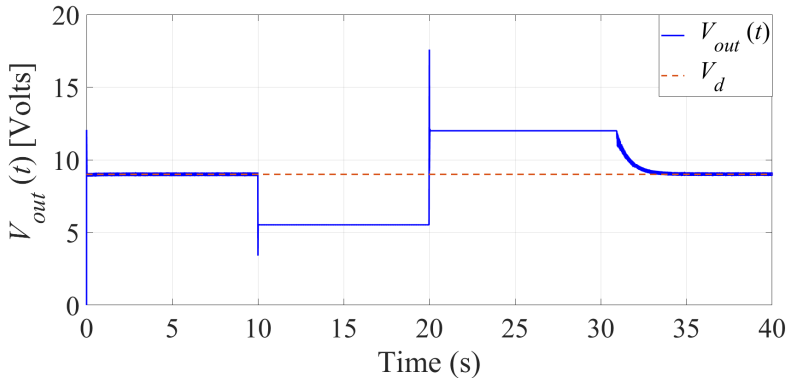

Figure 14. Scenario 2: Output voltage ($V_{out}(t)$) implementing a classical PID controller (simulation 2).

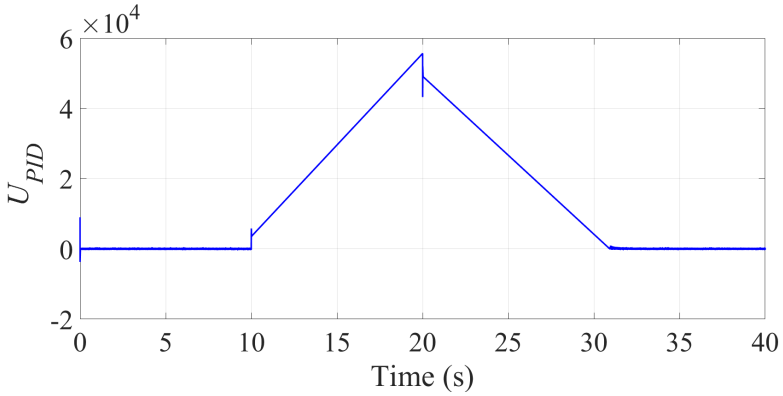

Figure 15. Scenario 2: Control input to generate the duty cycle of a PWM signal using a classical PID controller (simulation 2).

Finally, we implemented the proposed nonlinear PID controller using the same gains as those in scenario 1, as can be seen in Table 3. In Figure 16, we observe that the output voltage ($V_{out}(t)$) after $t = 20$ converges to the desired value without the windup effect, which appears when a classical PID controller is implemented, as depicted in Figure 14. The obtained results are: $RMSE_{V_{out}(t)} = 0.1169$ V, $SSE = 0.0628$ V and $ST = 0.0018$ s. In Figure 17, notice that the PWM signal duty cycle, generated by U_{NLPID}, has the same bound as the previous scenario. In general, the best performance of the closed-loop system is obtained by implementing the nonlinear PID controller.

In summary, the obtained $RMSE_{V_{out}(t)}$, SSE and ST values implementing the classical PID and nonlinear PID controller, given by Equations (2) and (21), respectively, in the buck converter system for scenario 2, are shown in Table 5. The main idea behind using the PID controller with different gains is to show that the windup effect appears even when the gains are relatively small. In this scenario, there are significant advantages of the proposed nonlinear PID controller, especially to avoid the windup effect in the output voltage.

Table 5. System performance for $20 < t$ in scenario 2.

Controller	$RMSE_{V_{out}(t)}$ (Volts)	SSE (Volts)	ST (s)
Classical PID (simulation 1)	1.5726	0.0499	15
Classical PID (simulation 2)	1.6126	0.0432	13
Nonlinear PID	0.1169	0.0628	0.0018

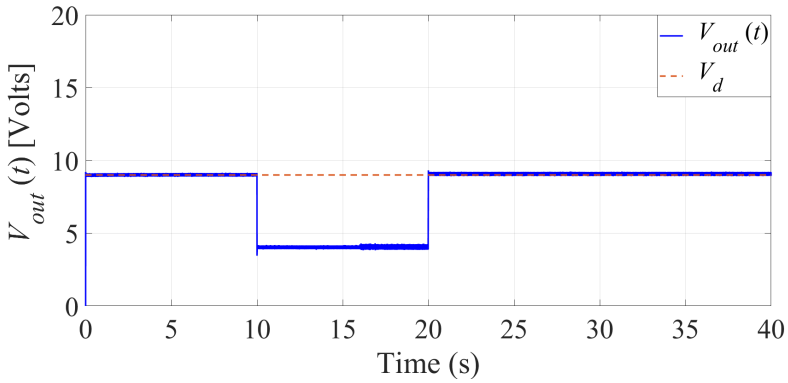

Figure 16. Scenario 2: Output voltage ($V_{out}(t)$) implementing the proposed nonlinear PID controller.

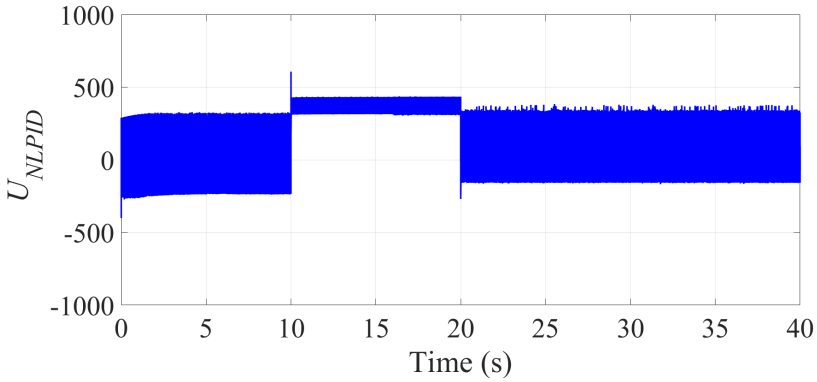

Figure 17. Scenario 2: Control input to generate the duty cycle of a PWM signal using the proposed nonlinear PID controller.

5. Experimental Results

For practicality reasons, we used an Arduino UNO target, as depicted in Figure 18, to implement the classical PID and the proposed nonlinear PID controllers; the pseudocode of the embedded algorithm for the experiments is presented in Algorithm 1. The components' values were computing as explained in Section 2; however, the values of L and C were adjusted to standard values of $L = 4.3 \times 10^{-3}$ H and $C = 2.2 \times 10^{-5}$ F, respectively.

Algorithm 1: Embedded algorithm to implement the control strategy.

Initiation:
1.- Define the frequency of PWM signal (5000 Hz)
2.- Define the gains k_p, k_i and k_d.
3.- Define the gains parameters b_1, b_2, b_3, d_1, d_2, d_3, μ_1, μ_2 and μ_3.
4.- Measure the input analogue voltage (V_{in}) and compute error value:
$e = V_d - V_{in}$
5.- Alfa-Beta filter to reduce the noise of e and estimate its derivative $(\dot{e})$.
6.- Estimate the integral value using the Sampling Period (SP):
$Inte = \sum(e * SP)$
7.- Choose the controller (1 or 2) to obtain the PWM value:
CASE 1: Classical PID controller, this is:
$PWM_{out} = k_p e + k_i Inte + k_d \dot{e}$
CASE 2: Nonlinear PID controller, this is:
Compute the variable gains $k_1(\cdot)$, $k_2(\cdot)$ and $k_2(\cdot)$ with:

$$k_1(\cdot) = \begin{cases} b_1|e|^{(\mu_1-1)} & if \quad |e| > d_1 \\ b_1 d_1^{(\mu_1-1)} & if \quad |e| \leq d_1 \end{cases}$$

$$k_2(\cdot) = \begin{cases} b_2|Inte|^{(\mu_2-1)} & if \quad |Inte| > d_2 \\ b_2 d_2^{(\mu_2-1)} & if \quad |Inte| \leq d_2 \end{cases}$$

$$k_3(\cdot) = \begin{cases} b_3|\dot{e}|^{(\mu_3-1)} & if \quad |\dot{e}| > d_3 \\ b_3 d_3^{(\mu_3-1)} & if \quad |\dot{e}| \leq d_3 \end{cases}$$

$$PWM_{out} = k_1(\cdot)e + k_2(\cdot)Inte + k_3(\cdot)\dot{e}$$

8.- Send PWM_{out} signal to MOSFET
9.- Acquire and save data responses in a text file
10.- If time $<$ 3600 s then **return to step 4**
11.-**END**

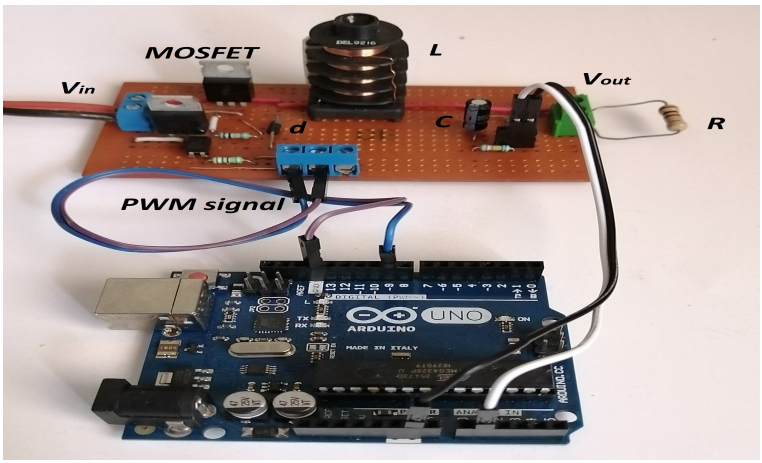

Figure 18. Buck converter experimental platform.

From the simulation results, notice that the main advantage of the proposed nonlinear PID controller is that in the case of scenario 2—therefore, for the experimental results, we only show this case. The gains for the classical PID and the nonlinear PID controllers were tuned again for the experimental implementation, as shown in Tables 6 and 7, respectively.

Table 6. Gains for a classical PID controller.

$k_1 = 700$	$k_2 = 900$	$k_3 = 0.07$

Table 7. Gains for a nonlinear PID controller.

For k_1	$b_1 = 250$	$d_1 = 0.2$	$\mu_1 = 0.1$
For k_2	$b_2 = 170$	$d_2 = 0.1$	$\mu_2 = 0.1$
For k_3	$b_3 = 0.1$	$d_3 = 0.1$	$\mu_3 = 0.9$

For the experiments, the input voltage was changed twice, first from 12 to 6 volts during approximately 10 s and after from 6 to 12 volts, as depicted in Figure 19. Then, the obtained output voltage implementing a classical PID controller was shown in Figure 20. Notice that the windup effect was presented as we obtained in the simulation results. The control input to generate the duty cycle of a PWM signal using a classical PID controller was shown in Figure 21. Notice that the duty cycle for the Arduino target was operated from 0 to 255.

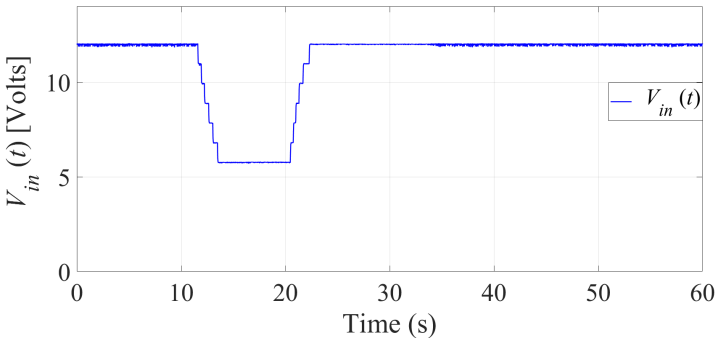

Figure 19. Input voltage $V_{in}(t)$ to test the closed-loop system implementing a classical PID controller.

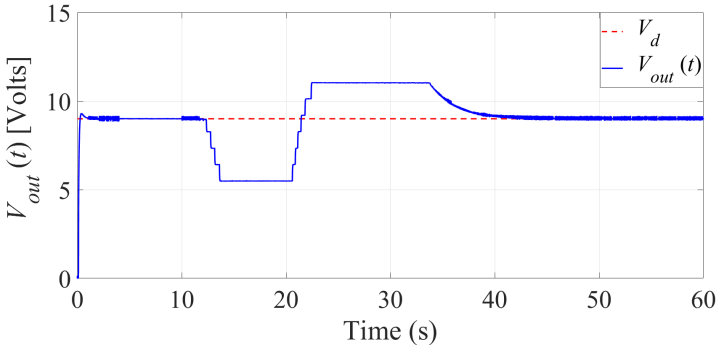

Figure 20. Desired voltage value (V_d) and performance of the output voltage ($V_{out}(t)$) implementing a classical PID controller.

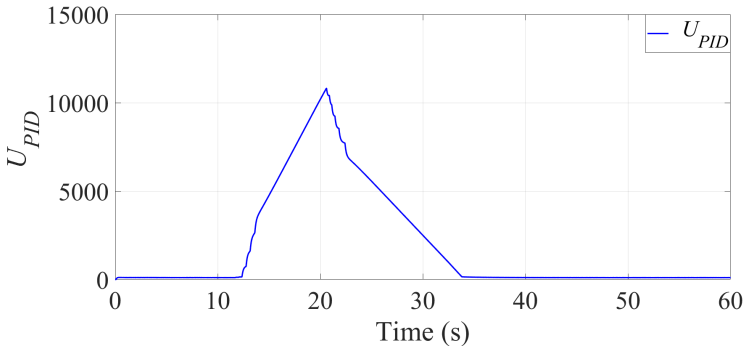

Figure 21. Control input produced by the classical PID controller to manipulate the duty cycle of a PWM signal.

The input variable voltages for the second experiment are shown in Figure 22, where we observe that the change in input voltage was manually performed in the mode moving the rotary switch knob. The obtained output voltage implementing the proposed nonlinear PID controller is shown in Figure 23, in which we note that the output voltage ($V_{out}(t)$) converges to the desired value without the windup effect; consequently, the proposed nonlinear controller does not allow wasting the energy in the buck converter system. The control input to generate the duty cycle of a PWM signal using the proposed nonlinear PID controller is shown in Figure 24.

Now, to observe the main advantage of the proposed controller, we compute the $RMSE_{V_{out}(t)}$, SSE and ST values before and during the disturbance. In Table 8, we show the obtained results for the classical PID and nonlinear PID controllers from 0 to 10 s, when the buck converter system is operating under nominal conditions. We note that, in this case, the obtained results are close for both controllers.

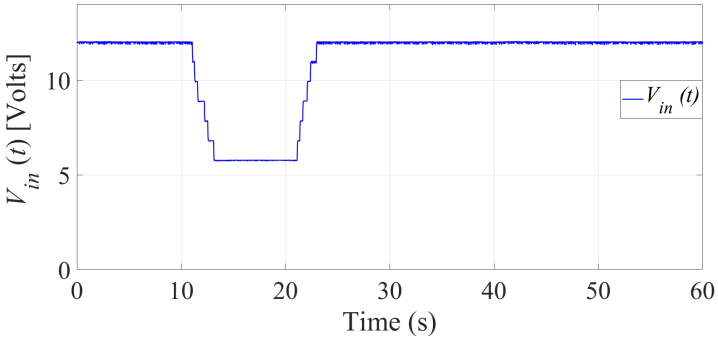

Figure 22. Input voltage $V_{in}(t)$ to test the closed-loop system implementing the proposed nonlinear PID controller.

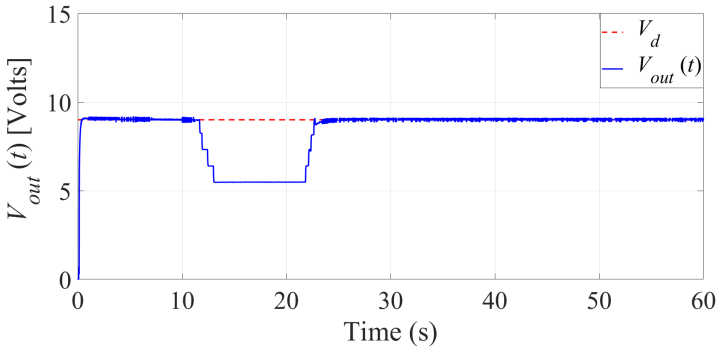

Figure 23. Desired voltage value (V_d) and performance of the output voltage ($V_{out}(t)$) implementing the proposed nonlinear PID controller.

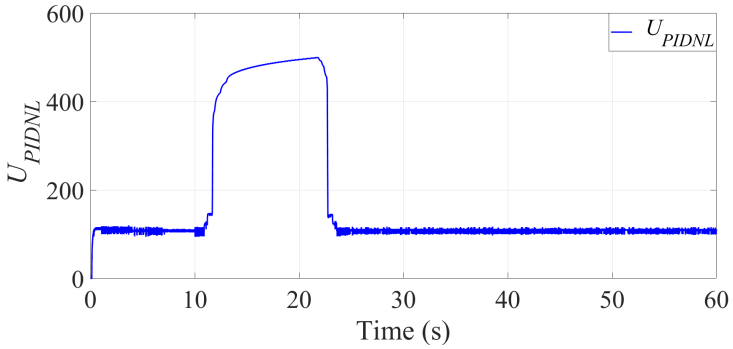

Figure 24. Control input produced by the proposed nonlinear PID controller to manipulate the duty cycle of a PWM signal.

Table 8. System performance before the voltage disturbance.

Controller	$RMSE_{V_{out}(t)}$ (Volts)	SSE (Volts)	ST (s)
Classical PID	1.004	0.0194	0.6
Nonlinear PID	1.065	0.0315	0.4

Finally, the obtained $RMSE_{V_{out}(t)}$, SSE and ST values computed during the disturbance, from 20 to 60, for the both controller, are shown in Table 9. With the obtained results, we can conclude that the proposed nonlinear PID controller improved the performance of the closed-loop system.

Table 9. System performance during the disturbance.

Controller	$RMSE_{V_{out}(t)}$ (Volts)	SSE (Volts)	ST (s)	Windup Effect
Classical PID	1.1543	0.0179	22	YES
Nonlinear PID	0.0270	0.0257	2	NO

6. Conclusions

The experiments and simulation results elucidated the robustness of the proposed nonlinear PID controller in the presence of a changing input voltage produced by renewable energy systems where the main energy source is not constant during the operation, as is the case in the photovoltaic and wind turbine low-power systems. In general, based on the obtained results, we can conclude that the performance of the nonlinear PID controller is acceptable from a practical point of view.

The main advantage of the proposed control strategy is to avoid the windup effect, which is normally produced by the integral term under some operation conditions, in this case, when the input voltage is less than the desired voltage for a relatively long time.

Notice that, in the obtained results, when implementing a classical PID controller, the windup effect appears even if we use relative small gains.

The main characteristic of the proposed nonlinear PID controller is the mathematical representation given by Equations (21)–(24). Observe that the proposed controller is relatively easy to implement in any embedded systems, given that the variable gains are computed with basic arithmetic operations.

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